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MEMS based digital variable capacitors with a high-*k* dielectric insulator

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Abstract

A novel MEMS based digital variable capacitor was designed and fabricated. The device consists of a multi-cantilever (or bridge) with variable length, suspended over a bottom electrode. By applying a voltage between the electrodes, the electrostatic force pulls the beams in one-by-one, realizing a digital increase in capacitance. A high-*k* dielectric HfO_2 is also introduced to increase the capacitance value and tuning range. These devices were fabricated by a four-mask process, and electrical tests have confirmed the stepwise increase of the capacitance with bias. However it was found that it is difficult to pull-in more than 10 cantilevers and most of the cantilevers remained on the substrate when the bias is off. Charge injection from the pulled-in electrode into the insulator increases the pull-in voltage drastically, and prevents pulling-in more cantilevers. Trapped charges in the insulator produce an electrostatic force and keep the cantilever stuck on the substrate.
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Keywords: MEMS; Digital variable capacitor; High-*k* dielectric; Charge injection

1. Introduction

Radio-frequency (RF) microelectromechanical systems (MEMS) is a technology that offers outstanding performance advantages over conventional solid-state devices, such as low power consumption, low insertion loss, high reliability and high quality factor. It is believed that RF-MEMS will be the next technology frontier, and revolutionize microelectronics industry. The MEMS based switches (dc- and ac-modes) and capacitors are the most important components for RF applications. They have a mechanical structure that isolates the control circuit from the signal circuit, and a mechanical inertia that prevents modulation of the capacitance value by RF signal, and provides good linearity. They have wide applications in microelectronics, mobile communications, and remote measurement and controls. There are two basic types of MEMS capacitors. One is the gap-tuning variable capacitor using two parallel plates horizontally positioned, and has a limited tuning distance up to a third of the gap [1]. The other one is the area tuning variable capacitor typically using a comb-drive structure which is normally made by deep reactive ion etch [2,3]. Both configurations have limited capacitance values, tuning ranges and difficulty of precision control of capacitance, thus limiting their applications. Attempts have been made to increase the capacitance and tuning range by various designs and technologies, and substantial progress has been achieved such as the combination of thermal and electrostatic actuator [4], two gap tuning, etc. [5,6], but problems still remain with these designs. There is a need to provide variable capacitors that are able to provide fixed values of capacitances for digital circuit applications [7–10]. Here we report the design and fabrication of a new type MEMS based, digital variable capacitor with a high-*k* dielectric material.

2. Theoretical analysis

Fig. 1 shows schematic drawings of the digital type variable capacitors. The first device consists of a bottom electrode covered with a thin insulator, and a freestanding electrode with multi-cantilevers with variable length. The second one has a freestanding top electrode with multi-beams which has a fixed length and are double-clamped on both ends, while the length of the bottom electrode varies to obtain a modulation of the capacitance by voltage. When a potential voltage is applied between

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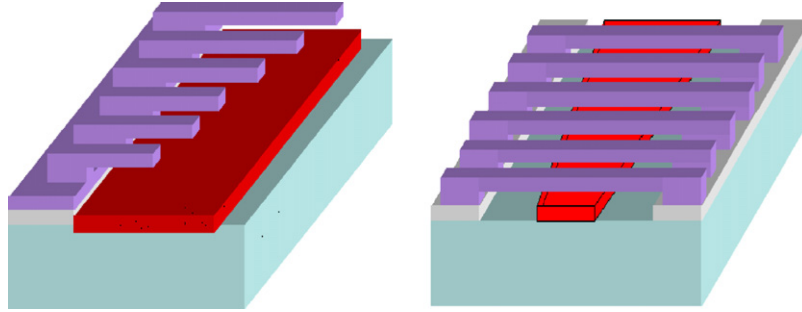

Fig. 1. Schematic drawing of variable capacitors with varying cantilever length (left) and varying bottom electrode length (right).

the bottom and top electrodes, an electrostatic force is generated, thus pulling in the cantilever (or bridge) beam. Further increasing the voltage, the longest cantilever beam eventually snaps down, and forms a capacitor with a thin insulator between the electrodes, leading to a step increase in capacitance. The capacitance is determined by the thickness of the insulator and its dielectric constant. Further increase of the voltage pulls-in the remaining cantilever beams one by one from long to short, realizing a step increase in capacitance. Ignoring the fringe effect and assuming the cantilevers are parallel to the bottom electrode, the pull-in voltage V_{th}^i (also called the threshold voltage) of the ith beam of a length L_i, is expressed as [11,12]:

$$V_{\mathrm{th}}^i = \sqrt{\frac{S_1 E t^3 y^3}{\varepsilon_0 L_i^3 Z}} \quad (1)$$

Here t is the thickness of the cantilever, y the gap, E the Young's modulus, ε_0 the permittivity in vacuum, Z the length of the bottom electrode and S_1 is a constant with a value of 0.28 for a freestanding cantilever [12], and 12 for a double-clamped beam [13]. The capacitance is dominated by the air gap when the cantilever is freestanding; while it is dominated by the thickness of the insulator when the beam is pulled-in. The capacitance of a cantilever beam is the sum of these two capacitors in series, and is expressed as

$$C_i = \frac{A_i k \varepsilon_0}{d\varepsilon_0 + yk} = \frac{L_i W_i k \varepsilon_0}{d\varepsilon_0 + yk} \quad (2)$$

Here d and k are the thickness and dielectric constant of the insulator, and A_i, L_i and W_i are the area, length and width of the ith cantilever beam. Since $yk \gg d\varepsilon_0$, a modulation of the gap by bias voltage before the beam is pulled-in makes little contribution to C_i, hence it can be treated as a constant. The total capacitance C, of a variable capacitor is the sum of the individual capacitors, C_i, when they are pulled-in. Assuming the cantilevers are in full contact with the insulator ($y \to 0$) when pulled-in, the total capacitance is then given by

$$C = \sum C_i = \sum \frac{L_i W_i k \varepsilon_0}{d\varepsilon_0 + yk} \approx \sum \frac{L_i W_i k}{d} \quad (3)$$

It is obvious from Eqs. (2) and (3) that a large value of capacitance and a large tuning range of a variable capacitor can be achieved by using a high-k dielectric material.

Fig. 2 shows the dependence of the capacitance on voltage for a multi-cantilever capacitor with k as a parameter. Here the thickness of the dielectric and the cantilever, and the gap were assumed to be 0.14, 1.6 and 1.6 μm, respectively. The cantilever length varies from 200 μm downwards with an interval of 5 μm and the beam width is fixed at 10 μm. The dielectric constants of 3.8, 7.8 and 20 correspond to those of SiO_2 and Si_3N_4 and HfO_2 insulators, respectively. The capacitance increases stepwise with bias and gradually saturates as the beam becomes shorter. It is obvious that at a fixed voltage a high capacitance can be obtained when a high-k insulator is used. A capacitor with HfO_2 insulator has a capacitance value five times higher than that with SiO_2 insulator.

From an application point of view, a linear relationship between the capacitance and voltage is most desirable, and great efforts have been made to achieve this, but at the cost of complicated configurations and processes [9,10]. The linear C–V relationship can be easily obtained from this digital variable capacitor by varying the width of the individual beam, as the pull-in voltage is not affected by the beam width significantly (ignoring the fringe effect) as indicated by Eq. (1). An example is shown in Fig. 2 by open circles, for a capacitor with the same cantilever beam length as others, but the width increases in $W_i = W_1(1 + 0.3i)$, here W_1 is the width of the first cantilever beam. The capacitance is linearly correlated to the voltage applied. This is impossible to be achieved from a single plate variable capacitor; and no special process is required, showing the superiority of this digital capacitor.

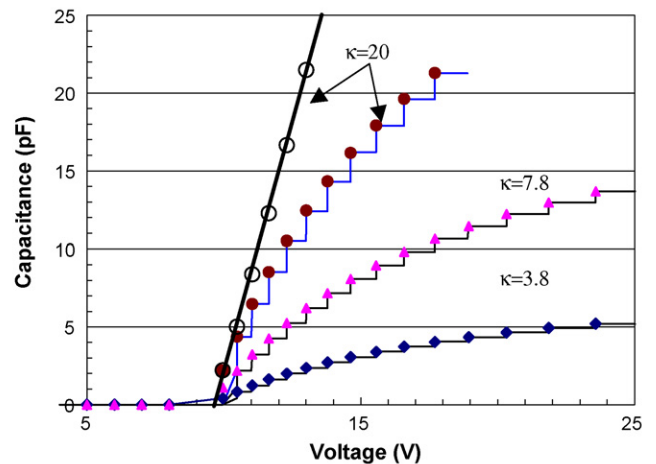

Fig. 2. Capacitance as a function of bias for a multi-cantilever variable capacitor with dielectric constant as a parameter. The open circles are calculated by varying the beam width.

When there is no internal stress in the thin film, the pull-in voltage for a double-clamped beam is the same as that expressed by Eq. (1) with a modified coefficient S_1. Therefore the capacitance of a bridge type digital capacitor has a similar function with respect to bias as shown in Fig. 2. However the length of the beam for the bridge type capacitors should be much longer to achieve a similar pull-in voltage. If there exists an internal stress in the film, the pull-in voltage for a double-clamped beam needs to be modified as follows [12,13]:

$$V_{\text{th}}^{i} = \sqrt{\frac{S_1 E t^3 y^3}{\varepsilon_0 L_i^3 Z} + \frac{S_2 t y^3 \sigma}{\varepsilon L^2}} \quad (4)$$

Here S_2 is a constant with value of 2.4 and σ is the internal stress of the thin film. A large compressive stress causes buckling of the beam, undesirable for device applications. A tensile stress is normally introduced in the film to prevent buckling of the double-clamped beam. The pull-in voltage increases drastically with the internal stress either in tensile or compressive. In some cases, the pull-in voltage becomes so high that causes a catastrophic breakdown of the dielectric when the electrode is pulled-in.

Based on these analyses, we have designed two sets of variable capacitors. One consists of multi-cantilevers with variable beam length, and the other one consists of multi-beams with a fixed length these are double-clamped. For comparison, we have also designed a number of variable capacitors with a single large cantilever or bridge on the same mask. For these large area devices, etch holes of 7 μm × 7 μm were introduced to reduce the release etch time.

3. Fabrication process

A four-mask process has been developed to fabricate these variable capacitors with process flow shown in Fig. 3. Note this is for proof of concept, the thickness of the substrate insulator, metallization and the guard-ring configuration are not optimized. SiO_2/Si wafers with a relatively thin oxide thickness of 1 μm were used which leads to a large stray capacitance with the substrate. A 0.2 μm thick Al was deposited by sputtering, patterned by standard photolithography and etched in an Al etchant to form the bottom electrode. Next step is the formation of the insulator on top of the bottom electrode. HfO_2 was chosen as the insulator and this too was formed by a lift-off process due to the etch difficulty. To achieve a better lift-off process, a photoresist (PR)/Cu double layer was developed. A Cu layer of ∼200 nm was sputtered, and patterned using PR 5214E. Then the exposed Cu was etched to form an undercut with the PR remaining on top of the Cu layer. A 140 nm thick HfO_2 was then deposited by sputtering. After removing the top PR in acetone, the remaining Cu layer was then etched by proprietary chromium etchant without attacking the Al electrodes. The samples were cleaned and loaded into the PECVD chamber for the deposition of the amorphous Si (*a*-Si) sacrificial layer up to a thickness of ∼1.6 μm. *a*-Si as a sacrificial layer has the advantages of fast deposition and etch rate, and low deposition temperature, and is a standard CMOS compatible material.

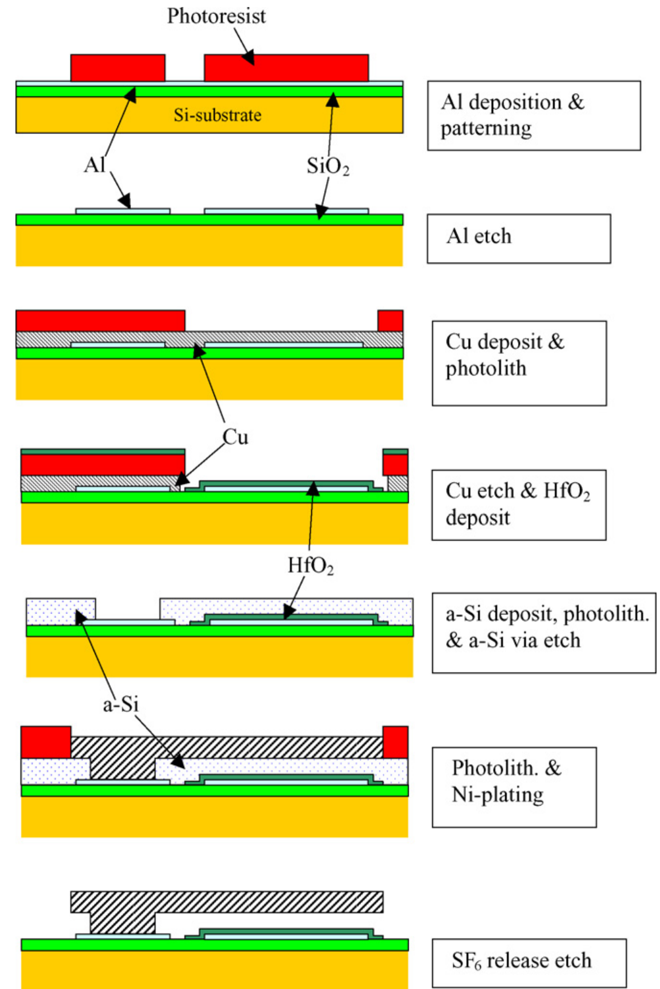

Fig. 3. The fabrication process flow.

The photolithography process to form via patterns was followed, and the *a*-Si was etched using SF_6 plasma. SF_6 plasma etch is an isotropic etch process, the etched vias have a nice slope, ensuring a total coverage for the subsequent seed layer for electroplating. A Cr/Cu seed layer (5/60 nm) was deposited by sputtering, and this was followed by photolithography using PR E5214 as a plating mould. The photoresist was spin coated at a speed of ∼2000 rpm to give a thickness of 2.5 μm. A Ni layer with a thickness of ∼1.6 μm was formed as the top electrode using the "through mask-electroplating" technique [14,15]. The electroplating was performed at the optimal conditions (J = 3 mA/cm^2 and T = 60 °C) to give Ni structures with minimum stress and highest elastic modulus [16,17]. Finally the top electrodes were released by removing the unwanted seed layer, and then the *a*-Si sacrificial layer was etched using SF_6 plasma.

Fig. 4 shows the optical photos of released cantilever (a) and bridge (b) type variable capacitors, and a large bridge type variable capacitor (c). Fig. 5(a) shows the details of the cantilevers with all beams held straight, indicating the gradient stress is minor in the electroplated Ni films. However for the bridge type capacitor, the beams buckled upwards in the middle, leading to a large gap between the top and bottom electrodes (Fig. 5(b)).

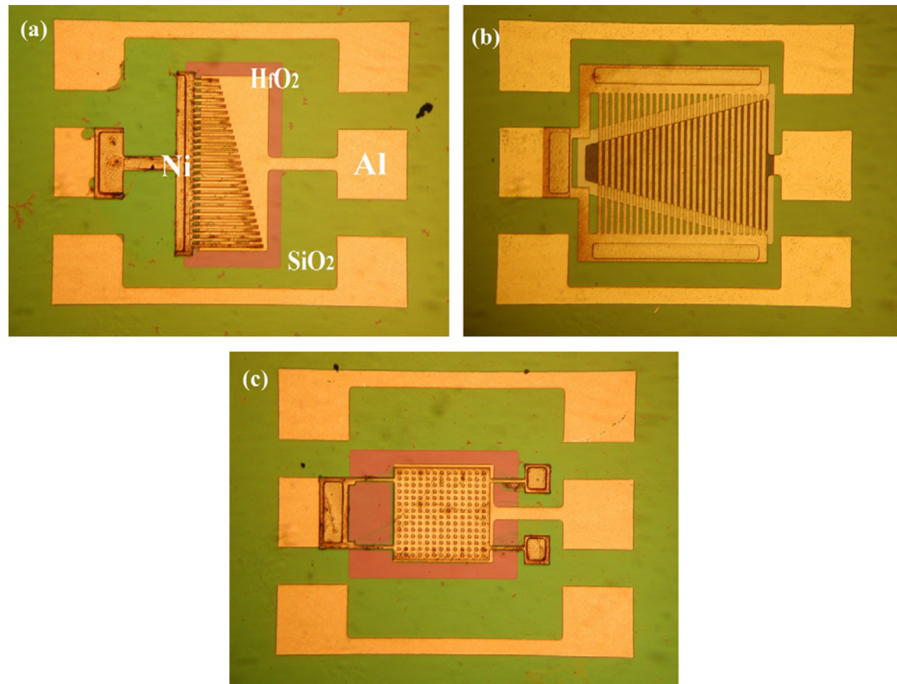

Fig. 4. Micro-photos of the variable capacitors with multi-cantilevers (a) and bridge beams (b) electrodes, and a large cantilever capacitor (c, $L \times W = 214\,\mu m \times 209\,\mu m$).

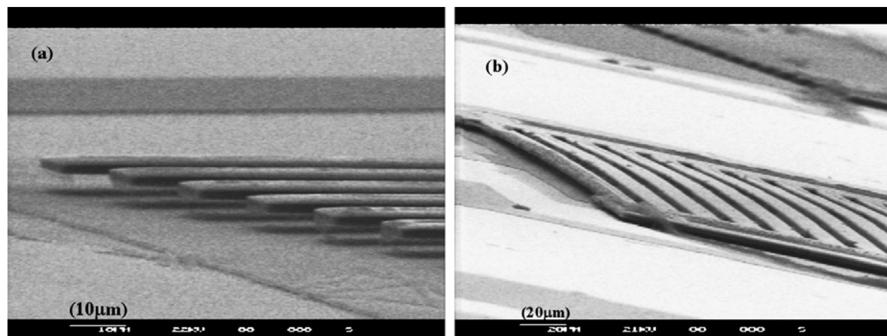

Fig. 5. SEM pictures of a cantilever (a) and a bridge type variable capacitors (b).

From previous work it is known that Ni-structures plated at 60 °C are under a minor tensile thermal stress [16,18], the compressive stress is more likely to be introduced during the release process. The typical time for the releasing etching was 10 min. A substantial temperature rise in the wafer is expected which may generate a large thermal expansion, leading to the plastic deformation. The shape of deformed beams remains after cooling. An improvement can be achieved by a timed release etch with periodic pausing for cooling. Fig. 6 shows the SEM picture of a single large cantilever capacitor with an area of $L \times W = 400\,\mu m \times 440\,\mu m$. The large cantilever held straight, again indicating a good Ni film without visible stress gradient.

4. Characterization and discussions

4.1. Single large plate capacitor

The capacitance was measured using a Boonton capacitance meter with an external voltage source. The voltage can be swept bi-directionally up to ±100 V, and a typical ramping step was 0.2 V. Fig. 7 shows the *C–V* characteristic of a single large cantilever capacitor with $L \times W = 300\,\mu m \times 440\,\mu m$. At low voltage, the capacitance increases slowly from ∼1.0 to 1.7 pF, corresponding to the gap tuning by bias voltage. At $V \sim 14$ V, a sudden increase in capacitance is obtained due to the pull-in of the large cantilever. The threshold voltage of ∼14 V is smaller than the theoretical value of ∼20 V and this is largely attributed to the fringe effects from the large number of etch holes. The capacitance increases with voltage, rather than remains at a fixed value. This behavior is believed to be caused by the angled contact of the cantilever with the bottom electrode when it is pulled-in. Further increasing the voltage pulls in the cantilever closer to the substrate, leading to a slow increase in capacitance. This behavior is more pronounced when the bias is ramped down. The capacitance decreases with the voltage, and returns to its original value at a voltage of 6 V as the cantilever returns to the freestanding position. A large hysteresis in the *C–V* characteristic is observed, and the width of the hysteresis varies from

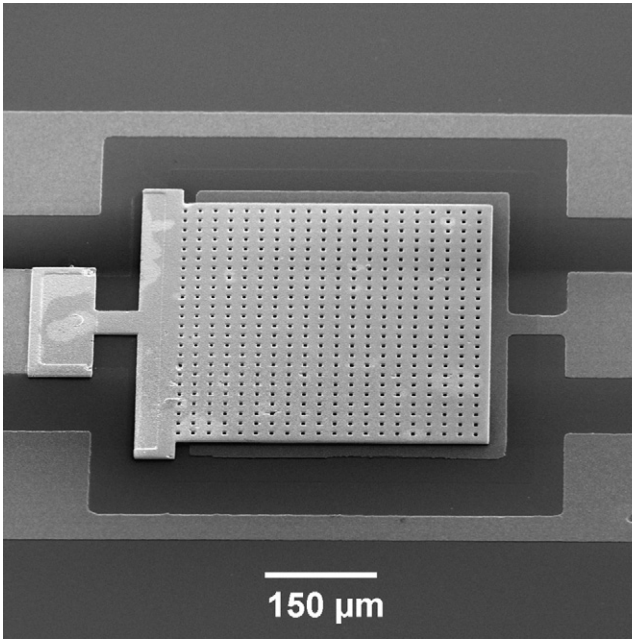

Fig. 6. An SEM picture of a large cantilever capacitor ($L \times W = 400\ \mu m \times 440\ \mu m$).

sample to sample in the range of 5–10 V. For such a large contact area, it is remarkable to have a hysteresis as small as ∼5 V, and it is believed that the insulator has effectively reduced the adhesion of the top electrode to the bottom electrode [19]. Fig. 8 shows the cantilever capacitance with device area as a variable. It is obvious that a large capacitance can be obtained using a large electrode.

When the voltage is swept in the negative direction, a similar *C–V* characteristic is obtained, but it is normally asymmetric along the $V = 0$ axis, indicating that charges exist in the insulator. Also the asymmetric characteristic becomes more severe when continuing to ramp-up the voltage after it is pulled-in for a long time. For instance, when biasing the pulled-in cantilever by a larger positive voltage, the pull-in voltage shifts in the positive direction. The threshold voltage can increase from ∼14 to 50 V depending on the time and voltage used for keeping the electrode

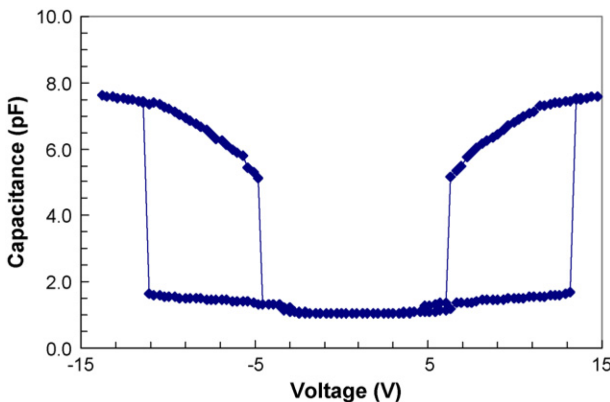

Fig. 7. A *C–V* characteristic of a large cantilever capacitor ($L \times W = 300\ \mu m \times 440\ \mu m$).

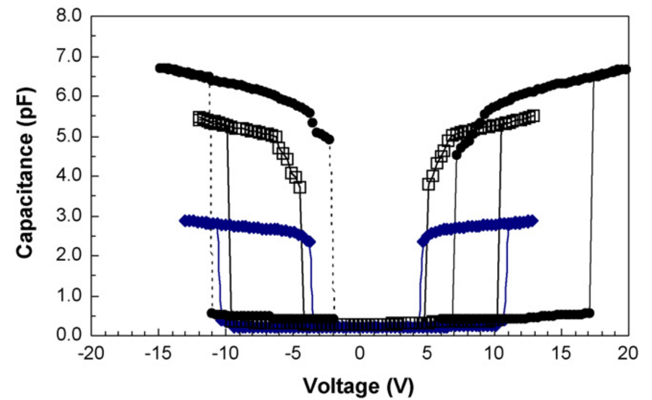

Fig. 8. *C–V* characteristics of large area, bridge type. The plate sizes are $L \times W$: 209 μm × 214 μm, 262 μm × 273 μm and 334 μm × 273 μm, respectively.

down. The charge injection at a high voltage and charge trapping in the insulator are believed to be responsible for this as will be discussed later.

4.2. Multi-cantilever capacitor

Fig. 9 shows the *C–V* characteristic of a digital variable capacitor with multi-cantilevers. In contrast to that of a single plate capacitor, the capacitance increases in step with the bias voltage, indicating that the cantilever beams are individually pulled-in. The voltage interval for individual beams to be pulled-in is not a constant, but varies from beam to beam. The magnitude of the first step rise in the capacitance is too large to correspond to a single cantilever beam. A close inspection under microscopy during measurement showed that three cantilevers were pulled-in simultaneously, leading to a big rise in capacitance. Although the device consists of 25 cantilever beams, it is difficult to pull-in more cantilevers after about 10 cantilevers being pulled-in. The *C–V* characteristic when ramping down the voltage is also shown in Fig. 9. Only two steps of decrease in capacitance were observed, and the capacitance remained almost unchanged with further decreasing the voltage. The cantilevers stuck on the substrate after the voltage is off.

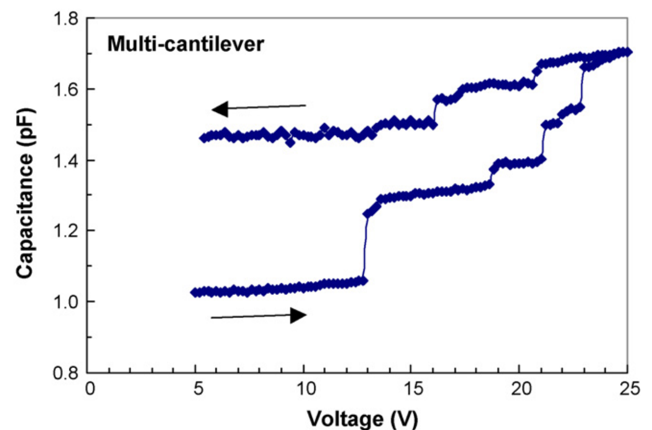

Fig. 9. A *C–V* characteristic of a multi-cantilever capacitor. The capacitance increases stepwise with voltage.

For the bridge type digital capacitor, it was found that the pull-in voltage is much higher than that of the multi-cantilever capacitor, typically $V_{th} > 50$ V. With such a high voltage, once the beam snaps down, a soaring electrical field causes a catastrophic breakdown of the insulator. The increased gap (Fig. 5) due to buckling caused by compressive stress in the Ni film is believed to be responsible for the increased pull-in voltage. Attempts are made to fabricate stress-free clamped beams to improve the characteristics of this type device.

4.3. Discussions

4.3.1. Charging effect

A number of abnormal phenomena was observed from the test devices: rapid increase in the threshold voltage, asymmetrical C–V along the $V = 0$ axis, and stiction of cantilevers on the substrate when the voltage is off. The charge injection into the insulator is believed to be responsible for these behaviors. The charging effect is one of the main reliability issues for ac-mode MEMS based RF-switches and capacitors, and has been studied intensively by many researchers [13,20,21].

When the electrodes are pulled-in, the electrical field across the insulator is several MV/cm, sufficient to cause the charge injection. The injected charges are trapped in the insulator, they screen off the bias voltage applied, increasing the threshold voltage. The amount of the shifted V_{th} is correlated to the number of injected charges though it normally has a broad distribution within the insulator. A detailed investigation revealed that the amount of the threshold voltage shifted (or charges injected) depends on the value of V_{th}, the continuity of the voltage ramp and ramping speed, and the time to keep the cantilever electrode on the substrate. In general, the longer the electrode contacts with the insulator, the more the threshold voltage shifts. The threshold voltage only shifts in one direction unless a reverse bias is applied, and it recovers slowly when the bias voltage is off. A full recovery of the threshold voltage takes hours even days, depending on the device temperature. Fig. 10 shows the shift of the C–V characteristics as a function of measurement cycle. A large shift in the threshold voltage was observed for the first switching cycle, as the voltage continued to ramp-up from 5 to 9 V after the electrode was pulled-in, and also the initial charging is normally much faster. For the second to fifth measurement cycles, the highest voltage to ramp down gradually increased from 9 to 11 V, providing a sufficient time for charging. The pull-in voltage shifts continuously but with a small amplitude compared to the first cycle.

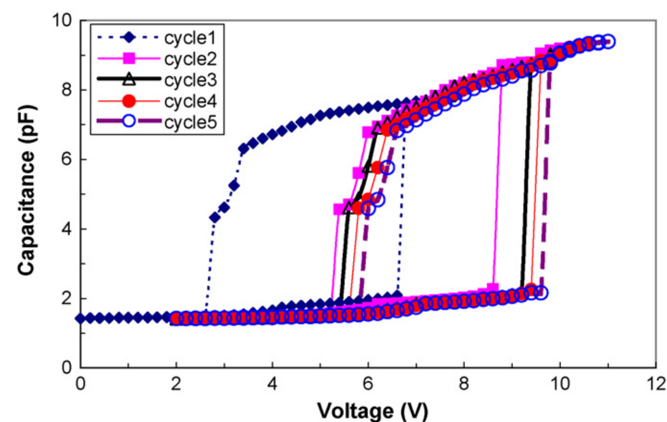

Fig. 10. C–V characteristics of a large cantilever capacitor as a function of measurement cycle, showing the shift of the pull-in voltage as the cycle increases.

The charging effect is responsible for the abnormal behaviors observed: the injected charges screen off the bias voltage, leading to a drastic increase in V_{th}, hence further increase in voltage is unable to pull more cantilevers as observed for multi-cantilever capacitor. An electrostatic force from the trapped charges holds the cantilevers on the substrate and prevents them to restore to their freestanding positions. Although a stepwise variation of capacitance has been realized using our proposed device configuration, they do not function as expected due to the charging effect. It should be avoided to apply a high voltage to the electrode of variable capacitor when it is pulled-in, hence a new structure configuration should be considered: instead of using a single bottom electrode, multi-bottom electrodes should be used to individually control the cantilever beams which are connected each other to provide a digital variable capacitance.

4.3.2. Small value of capacitances

The measured capacitance values are much smaller than those calculated using HfO_2 as an insulator, by a factor of 5–8 for all types of devices. The possible reasons are:

- Any residual particles or rough surfaces may introduce an extra gap between the electrodes, reducing the capacitance. However scanning electron microscopy (SEM) and atomic force microscopy measurements showed that the surface roughness is with in a few nanometers, it is unlikely to cause such a large decrease in capacitance.
- Additional insulators such as the Al and Cr oxide may be formed during processing. Also Cr and Cu may react with the *a*-Si sacrificial layer to form silicide or intermixing layer [22], a potential “semi-insulator”. Any additional layer will cause a drastic reduction of the capacitance. SEM measurement revealed an additional layer at the back of the cantilevers as shown in Fig. 11. Energy dispersive X-ray microanalysis measurement has been used to investigate the compositions of the cantilever back. Only Cr, Cu and Ni were detected, and no evidence was found for oxygen and Si. Therefore the step shown in Fig. 11 is more likely the Cr/Cu seed layer that may be formed by over-etch of the seed layer, but not other material. Nevertheless, the “step” increases the gap between the top and bottom electrodes, decreasing the overall capacitance.
- The capacitance was calculated based on two parallel plates with full contact, but the electrode could contact with the substrate at an angle or with a small contact area. Both of the cases reduce the capacitance significantly as schematically shown in Fig. 12. For devices with large gap and short beam length, the contact angle is much bigger; a much smaller capacitance is expected; while a long cantilever may contact with the substrate with a small area, the capacitance may reduce by a small amount, implying that the reduction factor will vary from sample to sample as observed.

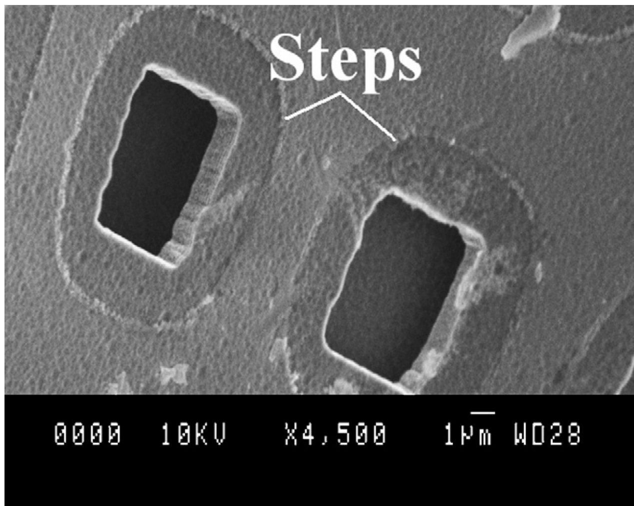

Fig. 11. An SEM picture of the cantilever back, showing an additional layer.

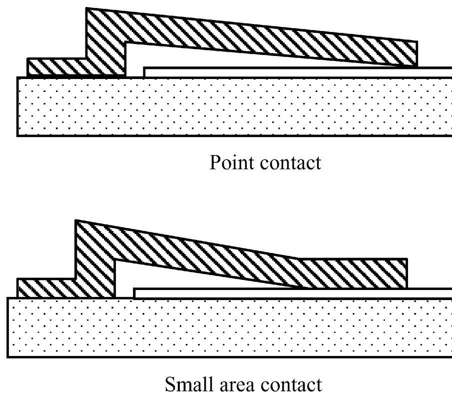

Fig. 12. A schematical drawing of an angled contact of the cantilever with the substrate, leading to a drastic decrease in capacitance.

5. Conclusions

MEMS based digital variable capacitors with multi-cantilevers and double-clamped beams were analyzed and designed. By applying the bias voltage between two electrodes, an increased electrostatic force pulls-in the cantilever beams one by one, realizing a digital increase in capacitance. A four-mask process was developed to fabricate these capacitors, and electrical tests were performed on these devices. The main results are summarized as follows:

1. Theoretical analysis revealed that a linear relationship between capacitance and voltage can be realized using this type of digital variable capacitors by varying the beam width.
2. Variable capacitors with a single large top electrode were obtained. It delivered a step change of capacitance up to 8 pF with a V_{th} lower than 15 V and a hysteresis of ∼5 V.
3. Digital variation in capacitance was realized from capacitors with multi-cantilevers. But it is difficult to pull-in more than 10 cantilevers, and most of cantilevers stick on the substrate when the voltage is off.
4. The charge injection into the insulator causes a dramatic increase in the threshold voltage which prevents the pull-in of more cantilevers, and also keeps them stuck on the substrate when the voltage is off.
5. All capacitors have a much smaller capacitance value than calculated. Detailed investigation showed no evidence of other additional layer formed at the back of the top electrodes. Angled contact of the pulled-in electrode with the substrate is responsible for the small value of the capacitances.

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